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| EXAMINER | |
|---|---|
| KNOLL, CLIFFORD H | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/920,825 | LEE, JIN WOO | |
| | Examiner | Art Unit | |
| | Clifford H. Knoll | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is responsive to communication filed 7/26/05. Currently claims 1-24 are pending.

### *Claim Rejections - 35 USC § 102*

1. *Claims 1-3, 5, and 7-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan (US 20010016920 A1).*

Regarding claim 1, Chan discloses an active module having a primary bus (e.g., Fig. 6, "225A", "266A") a CPU coupled to the primary bus (e.g., Fig. 4, "219A" via "225", see also Fig. 5A, "240A"), a primary arbiter coupled to the bus (e.g., Fig. 5A, "246A" which is seen arbitrating access through the agency of switches "290A", "292A", and "294A" (Fig. 6), the primary memory controller coupled to the primary bus that controls access to a primary memory coupled to the primary bus (e.g., Fig. 5A, "244A"), a primary D-channel controller separate from the primary memory controller and coupled to the primary bus (e.g., Fig. 5A, "250A") having a FIFO memory for the communication of parallel data on a duplexing path (e.g., Fig. 6, "229A"), and a primary C-channel controller separate from the D-channel controller (e.g., Fig 5A, "248A") and separate from the primary memory controller and coupled to the primary bus (e.g., Fig. 5A, "276A", "275A"), that communicates status information of the active module (e.g., Fig. 5A, "282A"), a standby module having a secondary bus (e.g., Fig. 6, "225B", "266B") a CPU coupled to the bus (e.g., Fig. 4, "219B" via "225"), a secondary arbiter coupled to the bus (e.g., Fig. 5B, "246B" which is seen arbitrating access through the agency of

switches "290B", "292B", and "294B" (Fig. 6), the secondary memory controller coupled to the secondary bus that controls access to a secondary memory coupled to the secondary bus (e.g., Fig. 5B, "244B"), a secondary D-channel controller separate from the secondary memory controller and coupled to the secondary bus (e.g., Fig. 5B, "250B") having a FIFO memory for the communication of parallel data on a duplexing path (e.g., Fig. 6, "229B"), and a secondary C-channel controller separate from the D-channel controller (e.g., Fig 5B, "248B") and separate from the secondary memory controller and coupled to the secondary bus (e.g., Fig. 5B, "276B", "275B"), that communicates status information of the secondary module (e.g., Fig. 5B, "282B"), a C-channel provided between the active and standby module that exchanges status information (e.g., Fig. 5A, "284A", "EXT_FAIL"), a D-channel, separate from the C-channel, provided between the active and standby module that supports access to primary and secondary memories by both primary and secondary processing units (e.g., Fig. 6, "294A", "294B", "290A", "290B").

Regarding claim 2, Chan also discloses wherein each of the primary and secondary C-channel controllers identifies the primary status information and the secondary status information, based on the values of a self-side active signal, a self-side normal signal, a pair-side active signal, and a pair-side normal signal, and determines which one of the active and standby modules is operating in an active mode and which is operating in a standby mode (e.g., paragraph [0047]).

Regarding claim 3, Chan also discloses the self-side active signal transmitted by the primary C-channel controller is designated as the pair-side active signal, when

received by the secondary C-channel controller; the self-side normal signal transmitted by the primary C-channel controller is designated as the pair-side normal signal, when received by the secondary C-channel controller; the self-side active signal transmitted by the secondary C-channel controller is designated as the pair-side active signal, when received by the primary C-channel controller (e.g., paragraph [0047]); and the self-side normal signal transmitted by the secondary C-channel controller is designated as the pair-side normal signal, when received by the primary C-channel controller (e.g., paragraph [0050]).

Regarding claim 5, Chan discloses reading a secondary status of a secondary module, via a C-channel, with a primary module, comparing the secondary status with a primary status of the primary module to obtain a first result, determining a direction of a D-channel based upon the value of the first result, and determining which one of the primary and secondary modules is an active module based upon the value of the first result (e.g., paragraph [0047]), reading only the contents of a first memory in the active module to a processor within the active module that requested the contents, when the processor performs a memory read operation of the first memory, and concurrently writing data to the first memory and to a second memory in the one of the primary and secondary modules that is not the active module and is, therefore, designated a standby module, when the processor performs a memory write operation (e.g., paragraph [0040]), and recognizing, with the standby module, that a fault has occurred in the active module by identifying an abnormal signal communicated by a C-channel controller of the active module, changing the active module to a standby mode of operation,

changing the standby module to an active mode of operation, changing the primary module or the secondary module that has the active mode of operation to be the active module, and changing the primary module or the secondary module that has the standby mode of operation to be the standby module (e.g., paragraph [0047]).

Regarding claim 7, Chan also discloses wherein step (b) further comprises: analyzing a transfer type signal and an address in a first D-channel controller of the active module to obtain a second result; if the second result is determined to be the memory read operation addressed to the first memory, reading the addressed contents only from the first memory and if the second result is determined to be either the memory write operation or the memory read operation addressed to the second memory, writing the address, the transfer type signal, and a transfer size signal from a first FIFO memory of the first D-channel controller to a second FIFO memory of a second D-channel controller of the standby module (e.g., paragraph [0066]); when an empty flag signal is asserted from the second FIFO memory, sending a bus request signal from the second D-channel controller to a bus arbiter of the standby module and receiving a bus grant signal at the second D-channel controller from the bus arbiter; after the bus grant signal is received, generating a transfer start signal from the second D-channel controller to a second memory controller of the standby module and transmitting the address to the second memory via an internal bus operation of the standby module; and if an operation completion signal is generated from the second memory controller, returning the bus grant signal to the bus arbiter (e.g., paragraph [0066], "slave data buffer 229B is not enabled until ...").

Regarding claim 8, Chan also discloses wherein the first FIFO memory writes the address, the transfer type signal and the transfer size signal to the second FIFO memory during the memory read operation (e.g., paragraph [0072], "address and control buffers 231, 233").

Regarding claim 9, Chan also discloses wherein the address determines whether the contents are read from the first memory or the second memory (e.g., paragraph [0072], "262B").

Regarding claim 10, Chan also discloses a first memory address region common to both the first memory and the second memory and a second address region used only for reading from the second memory (e.g., paragraph [0040], "224A has the capability to read from the remote memory 234B").

Regarding claim 11, Chan also discloses wherein the first D-channel controller recognizes both the memory read operation having the second region address and the transfer type signal and converts the second region address into a corresponding first region address and writes the corresponding first region address to the second FIFO memory (e.g., paragraph [0040], "executes the memory write concurrently").

Regarding claim 12, Chan also discloses wherein the first FIFO memory, at the time of the memory write operation, writes the address, the transfer type signal and the transfer size signal to the second FIFO memory and the second D-channel controller transmits the address via an internal bus of the standby module (e.g., paragraph [0040]).

Regarding claim 13, Chan also discloses if the memory read operation or the memory write operation is completed abnormally, the second D-channel controller inputs a transfer error acknowledge signal and asserts a D-channel error signal to the first D-channel controller, thereby generating a D-channel interrupt signal to the active module (e.g., paragraph [0051]).

Regarding claim 14, Chan also discloses if the memory read operation from the second memory is completed normally, the first D-channel controller communicates a primary transfer completion message to a first memory controller of the active module and the second D-channel controller communicates a secondary transfer completion message to the second memory controller (e.g., paragraph [0074]).

Regarding claim 15, Chan also discloses if the memory write operation to the second memory is completed normally, the second D-channel controller informs the first D-channel controller of a write completion (e.g., paragraph [0074]).

Regarding claim 16, Chan also discloses where step (c) further comprises: generating an interrupt in the active module, if the fault occurs; if the interrupt is generated in the active module, writing register information of a first D-channel controller, during a delay time, to a second FIFO memory of a second D-channel controller in a burst mode; if the write operation in the burst mode is completed, asserting a self-side abnormal status and a first self-side active status of the C-channel controller of the active module to a high state and transmitting an assert signal to the second D-channel controller; and asserting a second self-side active signal of the

standby module to a low state; and changing the standby module to the active mode of operation (e.g., paragraph [0077]).

Regarding claim 17, Chan discloses a first device and a second device of the duplex device each having a D-channel controller and a C-channel controller; a D-channel interconnecting the D-channel controllers of the first and second devices (e.g., Figure 4), to convey at least one of data signals, address signals, and control signals (e.g., Figure 6, "229A"); and a C-channel interconnecting the C-channel controllers of the first and second devices to convey status signals, wherein the C-channel controller of the first and second devices each monitor a subset of the C-channel status signals to determine which of the first and second devices has an active mode status and which has a standby mode status, and both the active mode status and the standby mode status are identified by a self-side normal signal and a pair-side active signal (e.g., paragraph [0047]).

Regarding claim 18, Chan also discloses the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal, and the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals (e.g., paragraph [0047]).

Regarding claim 19, Chan also discloses whichever one of the first and second devices has the active mode status, generates the address signals conveyed by the D-channel (e.g., paragraph [0044]).

Regarding claim 20, Chan also discloses each of the first and second devices share a common address bus and a common data bus and further comprises: a communication processor that communicates input and output I/O) information between the duplex device and external devices; a central processing unit that controls communication processes within the respective first and second devices; a memory that stores retained information; an arbiter that arbitrates the use of the common data bus, wherein one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to each memory of the first and second devices (e.g., Figure 6, paragraph [0033]).

Regarding claim 21, Chan also discloses within both of the first and second devices, respectively, the communication processor, the central processing unit, the memory, and the D-channel controller share the common data bus and the common address bus (Figure 6).

Regarding claim 22, Chan also discloses reading a first status of the first device and a second status of the second device; setting one of the first and second devices to an active mode status and the other of the respective devices to a standby mode status based on the first and second status, wherein both the first status and the second status are identified by a self-side normal signal and a pair-side active signal (e.g., paragraph [0047]).

Regarding claim 23, Chan also discloses the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-

side active signal, and the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals (e.g., paragraph [0047]).

Regarding claim 24, Chan also discloses the first and second devices each have a communication processing unit, a central processor, a memory, and a D-channel controller, which share both a common address bus and a common data bus; the first and second devices each have a C-channel controller that communicates with the central processor of the respective first and second devices; a D-channel interconnects the D-channel controllers of the first and second devices to convey data signals, address signals, and control signals; and a C-channel interconnects the C-channel controllers of the first and second devices to convey the first and second status between the first and second C-channel controllers, wherein one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to the memories of both the first and second devices (e.g., Figure 4).

***Claim Rejections - 35 USC § 103***

2. *Claims 4 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chan as applied to claims 3 and 5, respectively, above, and further in view of standard bus master embodiment, as further evidenced by of Shaffer (US 5884051).*

Regarding claim 4, Chan also discloses wherein each of the primary and secondary D-channel controllers obtains the primary status information and secondary status information, from the primary or secondary C-channel controller of its respective one of the active or standby modules and executes a duplexing operation, as a master or slave in a communication direction of the D-channel determined by a comparison of the primary status information and the secondary status information (e.g., paragraph [0045]). While Chan does not expressly mention a particular embodiment of the power PC (PPC) bus, the Examiner takes Official Notice that this is a well-known bus master standard as further evidenced by Shaffer. Shaffer discloses the well-known power PC bus (e.g., col. 4, lines 51-55, Figure 1). It would be obvious to combine the power PC bus with Chan, because the power PC bus is well-known bus master standard, and well recognized alternative embodiment of such. Therefore it would be obvious to one of ordinary skill in the art to combine a particular bus standard with Chan at the time the invention was made to obtain the claimed invention.

Regarding claim 6, Chan also discloses wherein the active module executes the memory write operation to the second memory, via the D-channel, and each of a primary D-channel controller and a secondary D-channel controller executes a duplexing operation (e.g., paragraph [0040]). While Chan does not expressly mention a particular embodiment of the power PC (PPC) bus, the Examiner takes Official Notice that this is a well-known bus master standard as further evidenced by Shaffer. Shaffer discloses the well-known power PC bus (e.g., col. 4, lines 51-55, Figure 1). It would be obvious to combine the power PC bus with Chan, because the power PC bus is well-

known bus master standard, and well recognized alternative embodiment of such. Therefore it would be obvious to one of ordinary skill in the art to combine a particular bus standard with Chan at the time the invention was made to obtain the claimed invention.

***Response to Arguments***

Applicant's arguments filed 7/26/05 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that Chan does not disclose "a primary central processing unit, a primary arbiter, a primary memory controller, a primary D-channel controller and a C-channel controller coupled to a primary bus" (p. 14); however, as the citations supra indicate, Chan discloses these features.

Applicant further argues that "[w]hile Chan may disclose a PCI bus 228A and a separate memory bus 230A (Fig. 4), this does not suggest the claimed features coupled to the primary bus" (p. 14); however Examiner finds that Chan's CPU is coupled to the separate memory bus 230A through the buffers "229A", "231A", "233A" (Fig. 4) via the coupling interface "240A" seen in Fig. 5A. Although the CPU does not directly arbitrate for use of this bus ("230A"), and subsequently is not directly connected to this bus as a bus agent is not distinguished by the claimed coupling, which the Examiner interprets as indicating that some form of connection, not necessarily direct, exists. The "PCI bus interface" of Fig. 5A is determined to be adequate to disclose the claimed coupling.

Applicant further argues that there is no "element of Chan ... corresponding to the claimed primary arbiter that arbitrates use of the primary bus (p. 14); however the arbiter as cited (Fig. 5A, "246A") arbitrates use of the primary bus "230A". Additional citation and notes are included in the rejection maintained supra for additional clarity.

Applicant further argues that "Chan's memory control logic unit 244A and arbitration logic unit 246A are provided within the first memory controller 224A and therefore cannot be considered separate from the memory controller 224A" (p. 14); however, this argument relies merely on the enclosure and terminology referred to in Fig. 5A as the "First Memory Controller 224A". The Examiner finds that the individual logic blocks of "224A" function separately, at least sufficiently to disclose the broadly claimed "separate" D-channel controller. Specifically, the "Memory Control Logic Unit 244A" discloses the memory controller. While it uses the same buffers that are provided by the D-channel controller, it is considered separate from the D-channel controller because "244A" provides access to the primary bus for the PCI bus interface, while the D-channel controller, through use of the "Bus Control Switch Unit 250A" provides access to the memory from the secondary controller. This differentiation in function is considered adequate to disclose the claimed "separate" nature of the D-channel controller.

Applicant further argues that "Chan's reset and fail logic unit 248A is clearly provided within the first memory controller 224A and therefore cannot be considered separate from the memory controller 224A" (p. 15); however, the issue of separateness has been treated supra; specifically, the enclosure of "248A" in the encompassing block

"224A" does not invalidate its separateness from the memory controller disclosed by Chan as "244A".

Regarding claim 17, Applicant argues that Chan does not disclose the features of the claimed invention (p. 15); however the citations above, not just that of paragraph 47, indicate those features relied upon in Chan. Specifically, Applicant argues that "the reset and fail logic unit 248A does not receive a self-side normal signal and a pair side active signal" (p. 16); however the Examiner relies on the "LOCAL_FAIL 282A" (Fig. 5A) signal, which, when inactive serves as the claimed "self-side normal signal", and on the "EXT_FAIL 284A" signal which, when inactive serves as the claimed "pair-side active signal". Both signals are sent over the C-channel, with the "LOCAL_FAIL 282A" appearing as "284B" in Fig. 5B.

Regarding claim 22, Applicant argues that Chan does not disclose "first status of the first device and the second status of the second device are both transmitted over the C-channel" (p. 17); however, this argument has been treated supra regarding claim 17.

Applicant further argues that Chan does not disclose "setting the devices based on first and second status both transmitted" (p. 17); however this apparently refers to the claimed "determin[ing] which of the first and second devices has an active mode status and which has a standby mode"; however, as Chan teaches, these signals are monitored to determine which device has an active mode (e.g., para. 51, "sole operation mode") and which has a standby mode, in this case, the absence of the "external fail signal" (para. 51).

Regarding claim 5, Applicant argues that Chan does not disclose "determining a direction of a D-channel based on a value of the first result" (p. 18); however, as Chan teaches, based upon a first result, in active mode "the memory controller 224 does not need to synchronize memory write accesses with the alternate I/O control unit" (para. 50). Examiner finds this discloses determining a direction, specifically, determining whether to send output to the alternate I/O control unit.

Applicant further argues that Chan does not disclose "reading only the contents of a first memory, and writing data to a first memory and to a second memory" (p. 18); however, in master mode (e.g., para. 47), the processor writes data to first and second memory (e.g., para. 50, the "need to synchronize memory write accesses with the alternate I/O control unit" when the alternate unit *is* "operational").

Thus the Examiner maintains the rejection.

## *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

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10/11/05